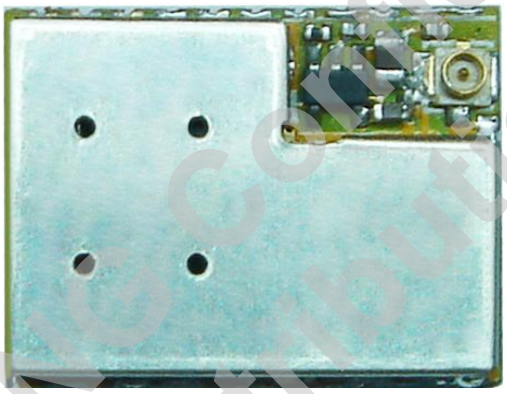
Wireless 2.4GHz 500mW Transceiver RF Module



Version History

Version	Date	Changes
V1.0	Feb. 22, 2012	1st. Edition

WENSHING **TRW-24HP** wireless 2.4GHz high power transceiver RF module is designed, developed and manufactured as contemplated for general use, without limitation, ordinary industrial use, general office use, personal use, and household use, but is not designed, developed and manufactured as contemplated

(1) For use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system).

(2) For use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

You shall not use this product for the above-mentioned using.

If your equipment is likely to be used for the above-mentioned uses, please consult with our sales representative before using.

WENSHING Component Division shall not be liable against you and/or any third party for any claims or damages arising in connection with the above-mentioned uses of this product.

Function Introduction

- **TRW-24HP** wireless 2.4GHz High power transceiver RF module is a frequency agile, half duplex.
- Transceiver is with SPI bus interface.
- Direct microprocessor
- Connection for control and data transfer eliminates.
- Needs for additional ICs, while integrated data code/decode hardware.
- Reduces the instruction set requirements on the associated microprocessor.
- Adjustable data rate, filter bandwidths and detection.
- Levels allow the IC to be used in a wide variety of high sensitivity/ High EMI environments. The **TRW-24HP** is ideally suitable for use in battery powered wireless applications in conjunction with Microprocessors for data communication.

Application

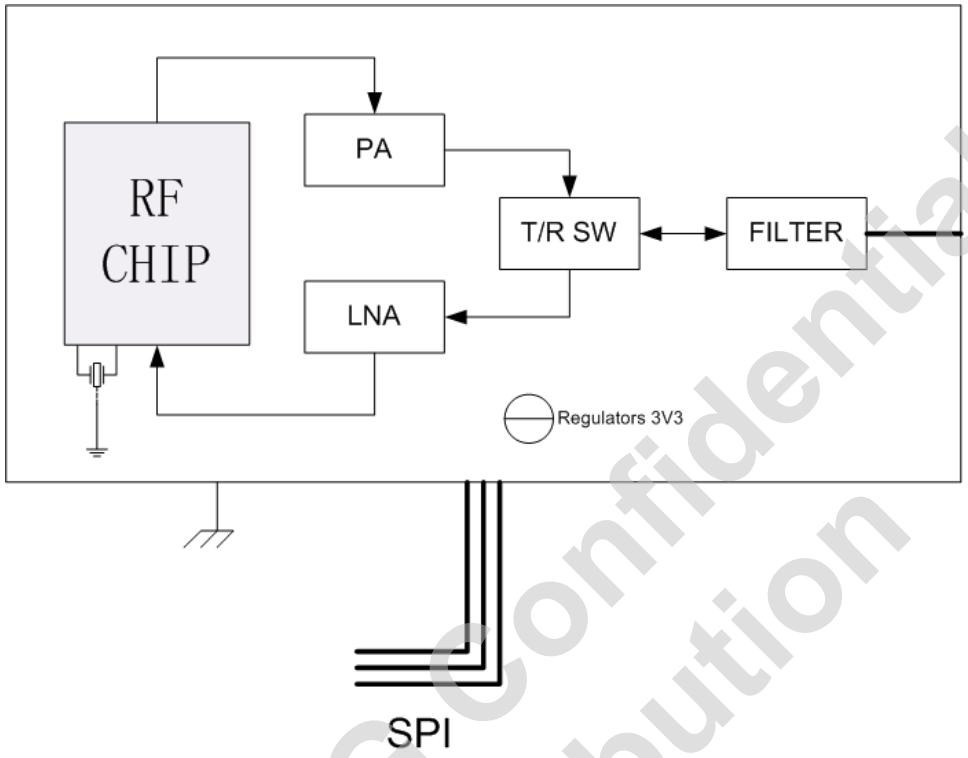
- Security System
- 2.4 GHz Cordless Phones
- Wireless Remote Control Car
- Wireless Remote Control Robot
- Automatic Power Switch Control
- Wireless Modem

Specification

- Frequency Range: 2.400GHz~2.4835GHz
- GFSK modulation
- Output Power: +27dBm 500mW (5V)
- Data Rates: from 1 to 2M bits/Sec
- Low Working Voltage: 3.7V~5.5V
- Input sensitivity: -95dBm(1MBPS)
- 3 separate 32 bytes TX and RX FIFOs
- Automatic Packet Handling
- RF Channels: 126
- Built-in Antenna connector
- RoHS Compliant

Parameter	Specification			Unit	Condition
	Min	Type	Max		
Frequency Range	2.4		2.4835	GHz	
Receiver Sensitivity	-98		-91	dBm	1Mbps
Data Rate	1		2	M Bit	GFSK
Supply Voltage, VDD	3.7		5.5	V	DC
TX Current		300		mA	
RX Current				mA	
Power down Current		1		uA	Power down Mode
standby-I mode Current		26		uA	standby-I mode
standby-II mode Current		360		uA	standby-II mode
Disable Current				uA	Enable PIN is LO
Power up time			100	ms	Disable to Enable time
Operating Temperature	-20		+70	°C	

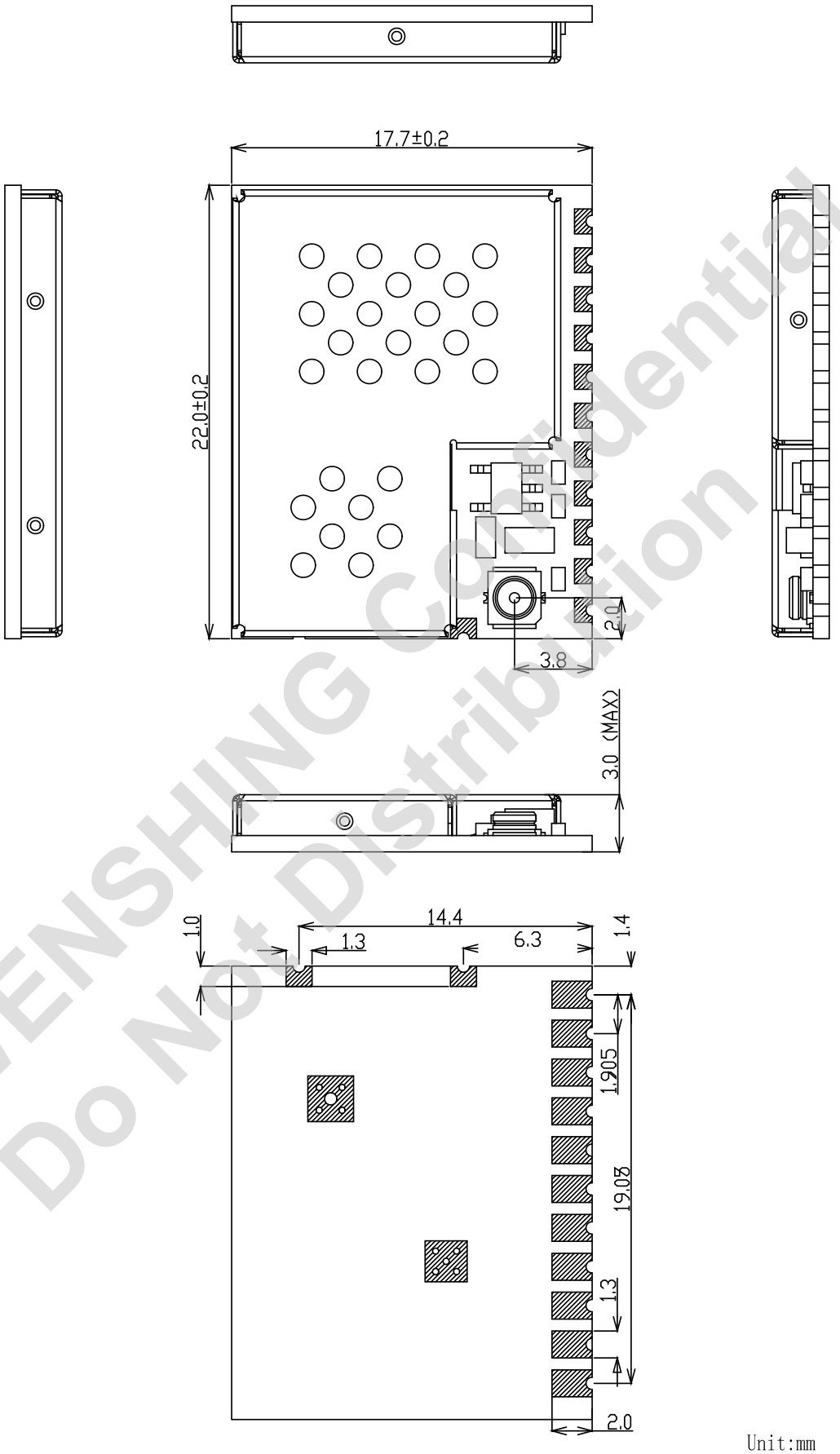
Internal Block Diagram



Absolute maximum ratings

Minimum	Maximum	Units	Operating conditions
Supply voltages			
-0.3	5.2	V	VDD
	0	V	GND
Input voltage			
-0.3	3.6	V	VI(DATA IN)
Output voltage			
GND TO 3	GND TO 3.3	V	VO

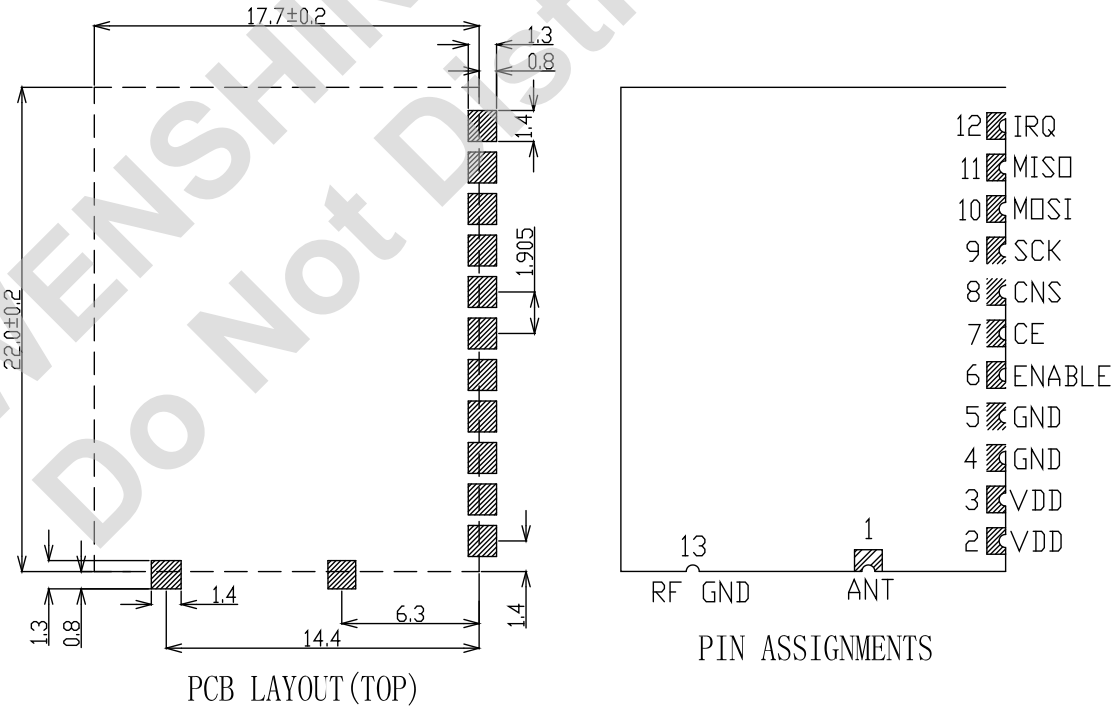
Size (unit: mm)



Unit:mm

Pin Assignment

Pin	Name	I/O	Description
1	Antenna	I/O	RF output to the antenna
2	VDD	POWER	Power Supply 3.7~5.5V
3	VDD	POWER	Power Supply 3.7~5.5V
4	GND	Ground	Ground
5	GND	Ground	Ground
6	ENABLE	I	Full power down 0 = full power down mode 1 = normal mode
7	CE	I	Chip Enable Activates RX or TX mode
8	CNS	I	SPI Chip Select
9	SCK	I	SPI Clock
10	MOSI	I	SPI Slave Data Input
11	MISO	O	SPI Slave Data Output
12	IRQ	O	Mask able interrupt pin. Active low
13	RF GND		RF Ground



Power Management

TRW-24HP has a IC regulator, external input power supply can be 3.7~5.5V input. When ENABLE Pin is on OL, module will not waste power. SPI interface can also declare a few powers saving mode:

- **Power down Mode**

Communicating thought SPI interface set PWR_UP REGISTER BIT to 0 in the module.

- **Standby –I Mode**

When set PWR_UP REGISTER BIT to 1, it enters Standby Mode. At the moment, the module's Crystal oscillation and wait for the next commend. This can shorten RF's start-up time during operation.

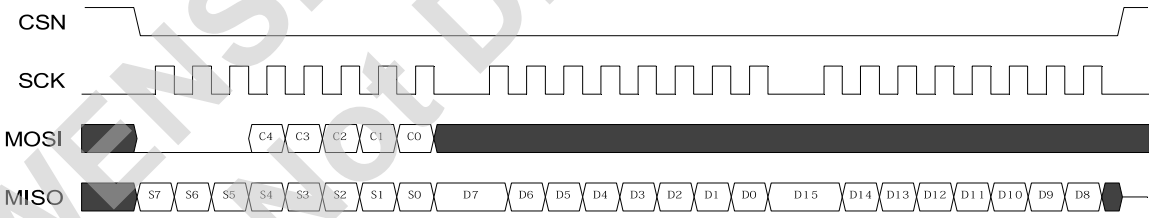
- **Standby –II Mode**

After setting PWR_UP REGISTER BIT to 1, Set Module's CE PIN to high potential. At the moment, FIFO data start to transmit, Module's PLL starts operating.

SPI Communication

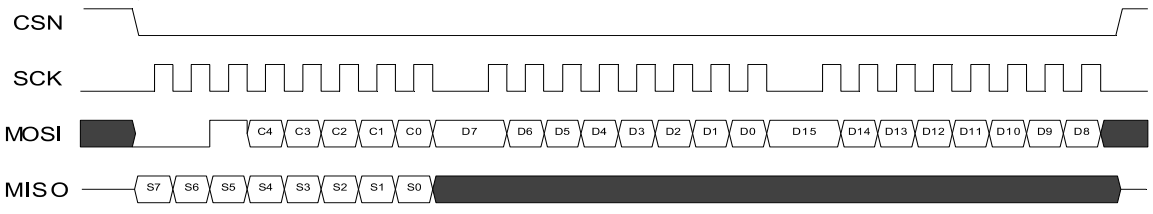
When MCU read REGISTER from RF Module, the diagram below is timing diagram. The first few bits are LO during read, because REGISTE address is not over 32. The writ method: When MCU is writing to RF Module, the fifth bit must be 1 to allow write.

SPI Read Timing diagram



SPI read operation

SPI Write Timing diagram



SPI write operation

REGISTER Description

Note: Register address 18H to 1BH is module testing sample,please to not use.

Address (Hex)	Flag	Bit	Reset State	Read/Write Type	Note 1 (REGISTER 8 bit)
00	**Function required to set module communication according to MCU**				
	Reserved	7	0	R/W	Only '0' allowed.
	MASK_RX_DR	6	0	R/W	Mask interrupt caused by RX_DR 1: Interrupt not reflected on the IRQ pin 0: Reflect RX_DR as active low interrupt on the IRQ pin.
	MASK_TX_DS	5	0	R/W	Mask interrupt caused by TX_DS 1: Interrupt not reflected on the IRQ pin 0: Reflect TX_DS as active low interrupt on the IRQ pin.
	MASK_MAX_RT	4	0	R/W	Mask interrupt caused by MAX_RT 1: Interrupt not reflected on the IRQ pin 0: Reflect MAX_RT as active low interrupt on the IRQ pin.
	EN_CRC	3	0	R/W	Enable CRC. Forced high if one of the bits in the EN_AA is high.
	CRCO	2	0	R/W	CRC encoding scheme '0' - 1 byte '1' – 2 bytes
	PWR_UP	1	0	R/W	1: POWER UP, 0:POWER DOWN
	PRIM_RX	0	0	R/W	RX/TX control 1: PRX, 0: PTX
01	**Enable 'Auto Acknowledgment' Function Disable this functionality to be compatible with nRF2401, see Note1**				
	Reserved	7:6	00	R/W	Only '00' allowed.
	ENAA_P5	5	1	R/W	Enable auto acknowledgement data pipe 5
	ENAA_P4	4	1	R/W	Enable auto acknowledgement data pipe 4
	ENAA_P3	3	1	R/W	Enable auto acknowledgement data pipe 3
	ENAA_P2	2	1	R/W	Enable auto acknowledgement data pipe 2
	ENAA_P1	1	1	R/W	Enable auto acknowledgement data pipe 1
	ENAA_P0	0	1	R/W	Enable auto acknowledgement data pipe 0
02	**EN_RXADDR Enabled RX Addresses**				
	Reserved	7:6	00	R/W	Only '00' allowed.

	ERX_P5	5	0	R/W	Enable data pipe 5
	ERX_P4	4	0	R/W	Enable data pipe 4
	ERX_P3	3	0	R/W	Enable data pipe 3
	ERX_P2	2	0	R/W	Enable data pipe 2
	ERX_P1	1	1	R/W	Enable data pipe 1
	ERX_P4	0	1	R/W	Enable data pipe 0
03					
	Reserved	7:2	000000	R/W	Only '000000' allowed.
	AW	1:0	11	R/W	RX/TX Address field width '00' - Illegal '01' - 3 bytes '10' - 4 bytes '11' – 5 bytes LSByte is used if address width is below 5 bytes.
04	**SETUP_RETR**	**Setup of Automatic Retransmission**			
	ARD	7:4	0000	R/W	Auto Retransmit Delay ‘0000’ – Wait 250µS ‘0001’ – Wait 500µS ‘0010’ – Wait 750µS…….. ‘1111’ – Wait 4000µS (Delay defined from end of transmission to start of next transmission).
	ARC	3:0	0011	R/W	Auto Retransmit Count ‘0000’ –Re-Transmit disabled ‘0001’ – Up to 1 Re-Transmit on fail of AA…… ‘1111’ – Up to 15 Re-Transmit on fail of AA
05	**RF_CH**	**RF Channel**			
	Reserved	7	0		Only '0' allowed.
	RF_CH	6:0	0000010	R/W	Sets the frequency channel nRF24L01 operates on.
06	**RF_SETUP**	**RF Setup Register**			
	Reserved	7:5	000	R/W	Only '000' allowed.
	PLL_LOCK	4	0	R/W	Force PLL lock signal. Only used in test.
	RF_DR	3	1	R/W	Air Data Rate ‘0’ – 1Mbps ‘1’ – 2Mbps
	RF_PWR	2:1	11	R/W	Set RF output power in TX mode '00' – -18dBm

					'01' – -12dBm '10' – -6dBm '11' – 0dBm
	LNA_HCURR	0	1	R/W	Setup LNA gain
07	**STATUS** **Status Register (In parallel to the SPI command word applied on the MOSI pin, the STATUS register is shifted serially out on the MISO pin)**				
	Reserved	7	0	R/W	Only '0' allowed.
	RX_DR	6	0	R/W	Data Ready RX FIFO interrupt. Asserted when new data arrives RX FIFOb. Write 1 to clear bit.
	TX_DS	5	0	R/W	Data Sent TX FIFO interrupt. Asserted when packet transmitted on TX. If AUTO_ACK is activated, this bit is set high only when ACK is received. Write 1 to clear bit.
	MAX_RT	4	0	R/W	Maximum number of TX retransmits interrupt Write 1 to clear bit. If MAX_RT is asserted it must be cleared to enable further communication.
	RX_P_NO	3:1	111	R	Data pipe number for the payload available for reading from RX_FIFO 000-101: Data Pipe Number 110: Not Used 111: RX FIFO Empty.
	TX_FULL	0	0	R	TX FIFO full flag. 1: TX FIFO full. 0: Available locations in TX FIFO.
08	**OBSERVE_TX**	**Transmit observe register**			
	PLOS_CNT	7:4	0	R	Count lost packets. The counter is overflow protected to 15, and discontinues at max until reset. The counter is reset by writing to RF_CH.
	ARC_CNT	3:0	0	R	Count retransmitted packets. The counter is reset when transmission of a new packet starts.
09	**CD**				
	Reserved	7:1	000000	R	device does not succeed to get packets through, as indicated by the MAX_RT IRQ for single packets and by the packet loss counter (PLOS_CNT) if several packets are lost. If the PLOS_CNT in the PTX device indicates a high rate of packet losses, the device can be configured to a PRX device

					for a short time (Tstbt2a +CD-filter delay = 130μs+128μs = 258μs) to check CD. If CD was high (jam situation), the frequency channel should be changed. If CD was low (out of range or jammed by broadband signals like WLAN), it may continue on the same frequency channel, but you must perform other adjustments (a dummy write to the RF_CH clears the PLOS_CNT)
	CD	0	0		
0A	RX_ADDR_P0	39:0	0xE7E7E7E7E7	R/W	Receive address data pipe 0. 5 Bytes maximum length. (LSByte is written first. Write the number of bytes defined by SETUP_AW)
0B	RX_ADDR_P1	39:0	0xC2C2C2C2C2	R/W	Receive address data pipe 1. 5 Bytes maximum length. (LSByte is written first. Write the number of bytes defined by SETUP_AW)
0C	RX_ADDR_P2	7:0	0xC3	R/W	Receive address data pipe 2. Only LSB. MSBytes is equal to RX_ADDR_P1[39:8]
0D	RX_ADDR_P3	7:0	0xC4	R/W	Receive address data pipe 3. Only LSB. MSBytes is equal to RX_ADDR_P1[39:8]
0E	RX_ADDR_P4	7:0	0xC5	R/W	Receive address data pipe 4. Only LSB. MSBytes is equal to RX_ADDR_P1[39:8]
0F	RX_ADDR_P5	7:0	0xC6	R/W	Receive address data pipe 5. Only LSB. MSBytes is equal to RX_ADDR_P1[39:8]
10	TX_ADDR	39:0	0xE7E7E7E7E7	R/W	Transmit address. Used for a PTX device only.(LSByte is written first) Set RX_ADDR_P0 equal to this address to handle automatic acknowledge if this is a PTX device with Enhanced ShockBurst™ enabled.
11	**RX_PW_P0**				
	Reserved	7:6		R/W	Only '00' allowed.
	RX_PW_P0	5:0		R/W	Number of bytes in RX payload in data pipe 0 (1to 32 bytes). 0 Pipe not used 1 = 1 byte… 32 = 32 bytes
12	**RX_PW_P1**				
	Reserved	7:6	00	R/W	Only '00' allowed.
	RX_PW_P1	5:0	00	R/W	Number of bytes in RX payload in data pipe 1 (1to 32 bytes).

					0 Pipe not used 1 = 1 byte… 32 = 32 bytes
13	**RX_PW_P2**				
	Reserved	7:6	00	R/W	Only '00' allowed.
	RX_PW_P2	5:0	0	R/W	Number of bytes in RX payload in data pipe 2 (1to 32 bytes). 0 Pipe not used1 = 1 byte… 32 = 32 bytes
14	**RX_PW_P3**				
	Reserved	7:6	00	R/W	Only '00' allowed.
	RX_PW_P3	5:0	0	R/W	Number of bytes in RX payload in data pipe 3 (1to 32 bytes). 0 Pipe not used 1 = 1 byte… 32 = 32 bytes
15	**RX_PW_P4**				
	Reserved	7:6	00	R/W	Only '00' allowed.
	RX_PW_P4	5:0	0	R/W	Number of bytes in RX payload in data pipe 4 (1to 32 bytes). 0 Pipe not used 1 = 1 byte… 32 = 32 bytes
16	**RX_PW_P5**				
	Reserved	7:6	00	R/W	Only '00' allowed.
	RX_PW_P5	5:0	0	R/W	Number of bytes in RX payload in data pipe 5 (1to 32 bytes). 0 Pipe not used 1 = 1 byte… 32 = 32 bytes
17	**FIFO_STATUS**	**FIFO Status Register**			
	Reserved	7	0	R/W	Only '0' allowed.
	TX_REUSE	6	0	R	Reuse last transmitted data packet if set high. The packet is repeatedly retransmitted as long as **CE** is high. TX_REUSE is set by the SPI command REUSE_TX_PL, and is reset by the SPI commands W_TX_PAYLOAD or FLUSH TX
	TX_FULL	5	0	R	TX FIFO full flag. 1: TX FIFO full. 0: Available locations in TX FIFO
	TX_EMPTY	4	1	R	TX FIFO empty flag 1: TX FIFO empty 0: Data in TX FIFO

	Reserved	3:2	00	R/W	Only '00' allowed.
	RX_FULL	1	0	R	RX FIFO full flag 1: RX FIFO full 0: Available locations in RX FIFO
	RX_EMPTY	0	1	R	RX FIFO empty flag 1: RX FIFO empty 0: Data in RX FIFO
N/A	ACK_PLDc	255:0	X	W	Written by separate SPI command ACK packet payload to data pipe number PPP given in SPI command Used in RX mode only Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled first in first out.
N/A	TX_PLD	255:0	X	W	Written by separate SPI command TX data payload register 1 - 32 bytes. This register is implemented as a FIFO with three levels. Used in TX mode only.
N/A	RX_PLD	255:0	X	R	Read by separate SPI command RX data payload register. 1 - 32 bytes. This register is implemented as a FIFO with three levels. All RX channels share the same FIFO
1C	**DYNPDc Enable dynamic payload length**				
	Reserved	7:6	0	R/W	Only '00' allowed.
	DPL_P5	5	0	R/W	Enable dyn. payload length data pipe 5. (Requires EN_DPL and ENAA_P5)
	DPL_P4	4	0	R/W	Enable dyn. payload length data pipe 4. (Requires EN_DPL and ENAA_P4)
	DPL_P3	3	0	R/W	Enable dyn. payload length data pipe 3. (Requires EN_DPL and ENAA_P3)
	DPL_P2	2	0	R/W	Enable dyn. payload length data pipe 2. (Requires EN_DPL and ENAA_P2)
	DPL_P1	1	0	R/W	Enable dyn. payload length data pipe 1. (Requires EN_DPL and ENAA_P1)
	DPL_P0	0	0	R/W	Enable dyn. payload length data pipe 0. (Requires EN_DPL and ENAA_P0)
1D	**FEATUREc Feature Register**				
	Reserved	7:3	0	R/W	Only '00000' allowed.
	EN_DPL	2	0	R/W	Enables Dynamic Payload Length.
	EN_ACK_PAYd	1	0	R/W	Enables Payload with ACK
	EN_DYN_ACK	0	0	R/W	Enables the W_TX_PAYLOAD_NOACK command.

Enhanced ShockBurst™ Transmitting Payload

1. The configuration bit PRIM_RX has to be low.
2. When the application MCU has data to transmit, the address for the receiving node (TX_ADDR) and payload data (TX_PLD) has to be clocked into nRF24L01 through the SPI. The width of TXpayload is counted from number of bytes written into the TX FIFO from the MCU. TX_PLD must be written continuously while holding **C**SN low. TX_ADDR does not have to be rewritten if it is unchanged from last transmit. If the PTX device shall receive acknowledge, data pipe 0 has to be configured to receive the ACK packet. The RX address for data pipe 0 (RX_ADDR_P0) has to be equal to the TX address (TX_ADDR) in the PTX device. For the example in Figure 1

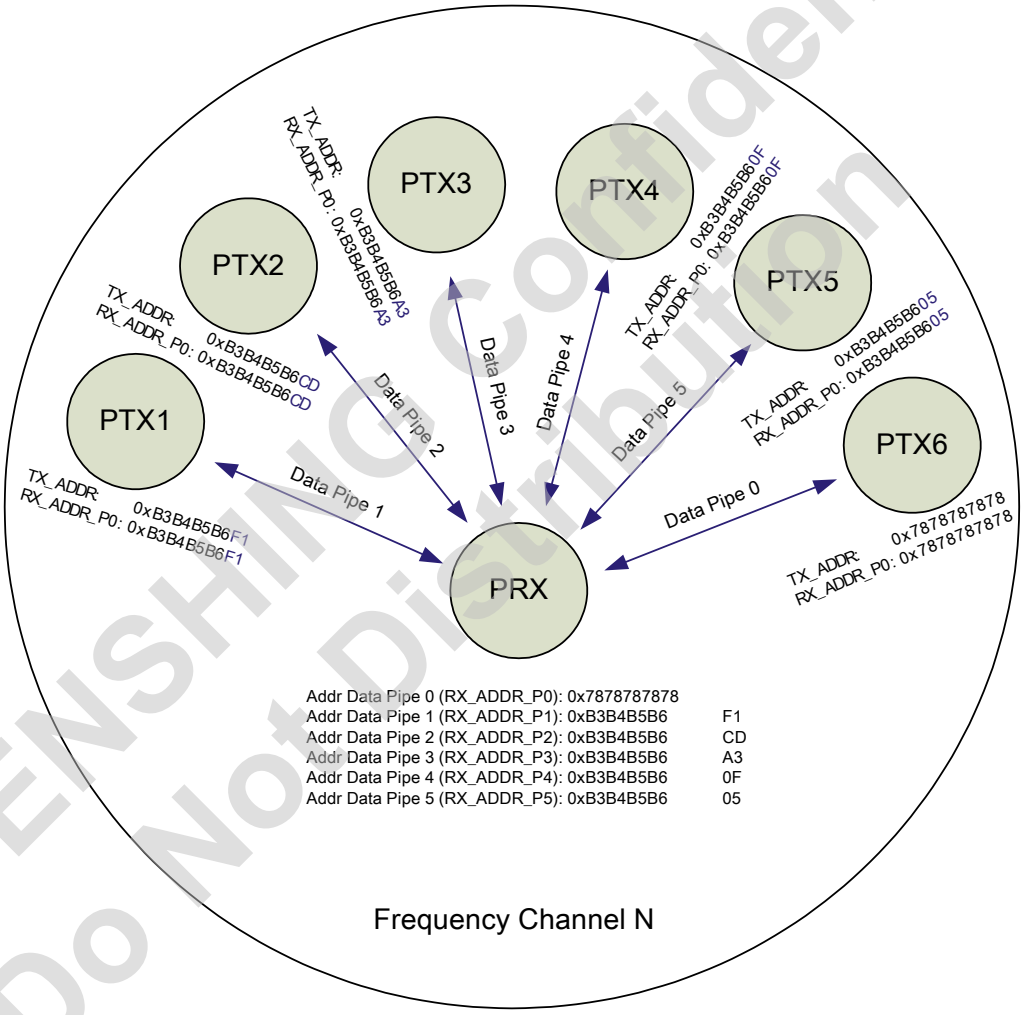


Figure 1

the following address settings have to be performed for the TX5 device and the RX device:

TX5 device: `TX_ADDR` = 0xB3B4B5B605

TX5 device: `RX_ADDR_P0` = 0xB3B4B5B605

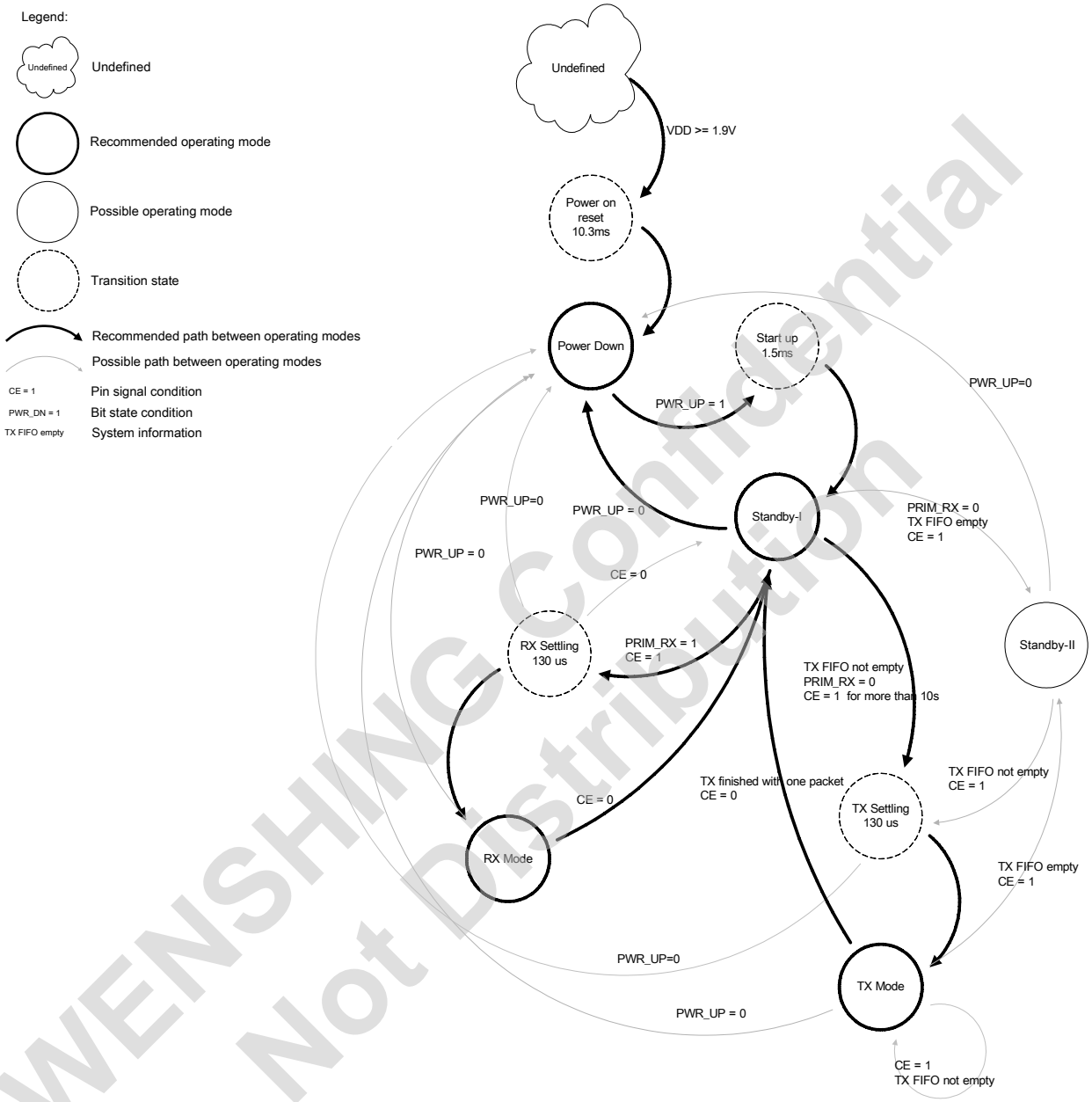
RX device: `RX_ADDR_P5` = 0xB3B4B5B605

3. A high pulse on **CE** starts the transmission. The minimum pulse width on CE is 10µs.
4. nRF24L01 ShockBurst™:
   - Radio is powered up.
   - 16MHz internal clock is started.
   - RF packet is completed (see the packet description).
   - Data is transmitted at high speed (1Mbps or 2Mbps configured by MCU).
5. If auto acknowledgement is activated (ENAA_P0=1) the radio goes into RX mode immediately, unless the NO_ACK bit is set in the received packet. If a valid packet has been received in the valid acknowledgement time window, the transmission is considered a success. The TX_DS bit in the STATUS register is set high and the payload is removed from TX FIFO. If a valid ACK packet is not received in the specified time window, the payload is retransmitted (if auto retransmit is enabled). If the auto retransmit counter (ARC_CNT) exceeds the programmed maximum limit (ARC), the MAX_RT bit in the STATUS register is set high. The payload in TX FIFO is NOT removed. The **IRQ** pin is active when MAX_RT or TX_DS is high. To turn off the IRQ pin, the interrupt source must be reset by writing to the STATUS register (see Interrupt chapter). If no ACK packet is received for a packet after the maximum number of retransmits, no further packets can be transmitted before the MAX_RT interrupt is cleared. The packet loss counter (PLOS_CNT) is incremented at each MAX_RT interrupt. That is, ARC_CNT counts the number of retransmits that was required to get a single packet through. PLOS_CNT counts the number of packets that did not get through after maximum number of retransmits.
6. nRF24L01 goes into standby-I mode if **CE** is low. Otherwise next payload in TX FIFO is transmitted. If TX FIFO is empty and **CE** is still high, nRF24L01 enters standby-II mode.
7. If nRF24L01 is in standby-II mode, it goes to standby-I mode immediately if **CE** is set low.

Enhanced ShockBurst™ Receive Payload

1. RX is selected by setting the PRIM_RX bit in the CONFIG register to high. All data pipes that receive data must be enabled (EN_RXADDR register), auto acknowledgement for all pipes running Enhanced ShockBurst™ has to be enabled (EN_AA register), and the correct payload widths must be set (RX_PW_Px registers). Addresses have to be set up as described in item 2 in the Enhanced ShockBurst™ transmit payload chapter above.
2. Active RX mode is started by setting CE high.
3. After 130µs nRF24L01 is monitoring the air for incoming communication.
4. When a valid packet has been received (matching address and correct CRC), the payload is stored in the RX-FIFO, and the RX_DR bit in STATUS register is set high. The **IRQ** pin is active Revision 2.0 Page 66 of 74 when RX_DR is high. RX_P_NO in STATUS register indicates what data pipe the payload has been received in.
5. If auto acknowledgement is enabled, an ACK packet is transmitted back, unless the NO_ACK bit is set in the received packet. If there is a payload in the TX_PLD FIFO, this payload is added to the ACK packet.
6. MCU sets the **CE** pin low to enter standby-I mode (low current mode).
7. MCU can clock out the payload data at a suitable rate through the SPI.
8. nRF24L01 is now ready for entering TX or RX mode or power down mode.

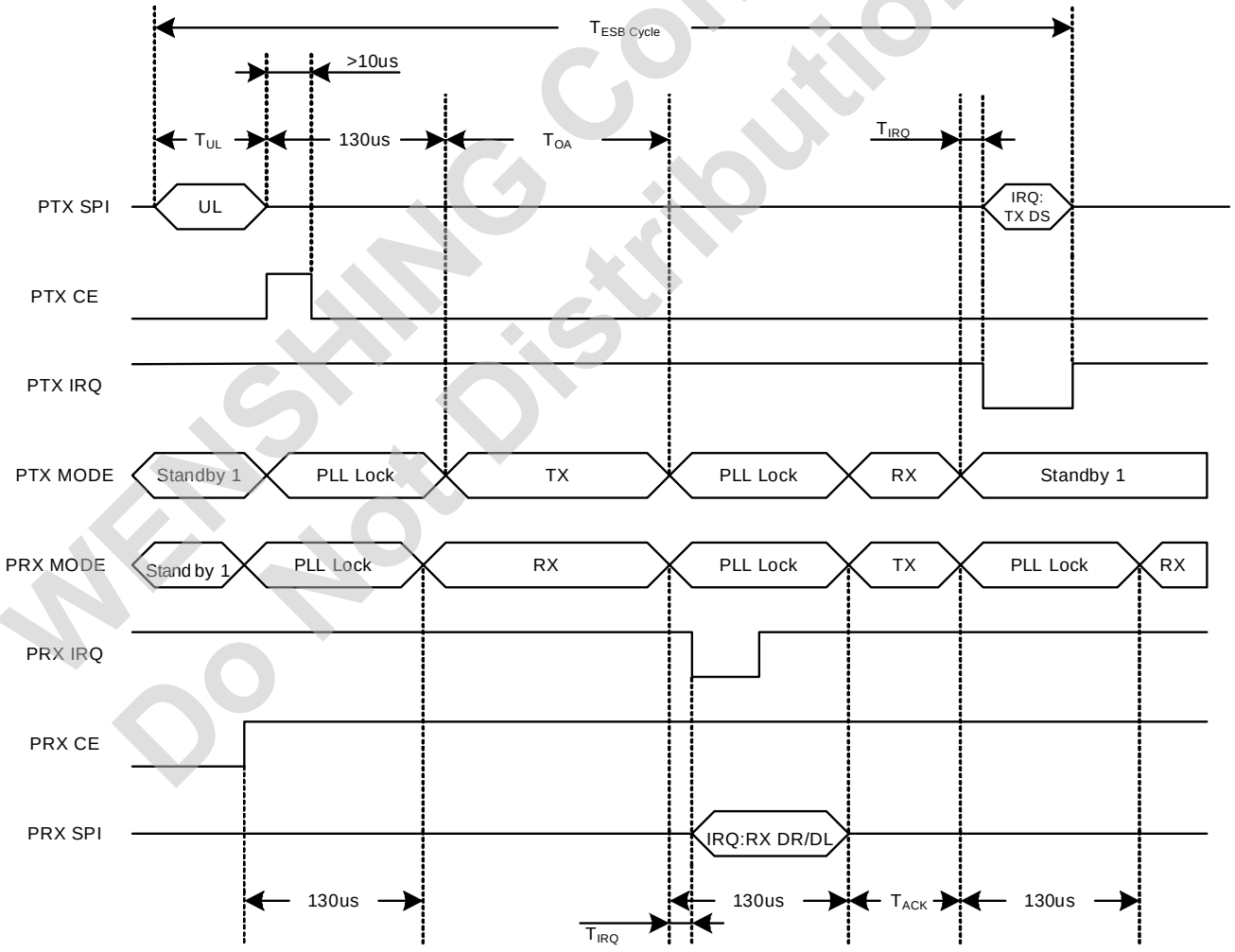
State Diagram



Radio control state diagram

Communication Example 1: When transferring date to 2.4GHz, the Length is XX; REGISTER is shown from table below:

Address	00	01	02	03	04	05	06	07
Data								
Address	08	09	0A	0B	0C	0D	0E	0F
Data								
Address	10	11	12	13	14	15	16	17
Data								
Address	18	19	1A	1B	1C	1D		
Data								

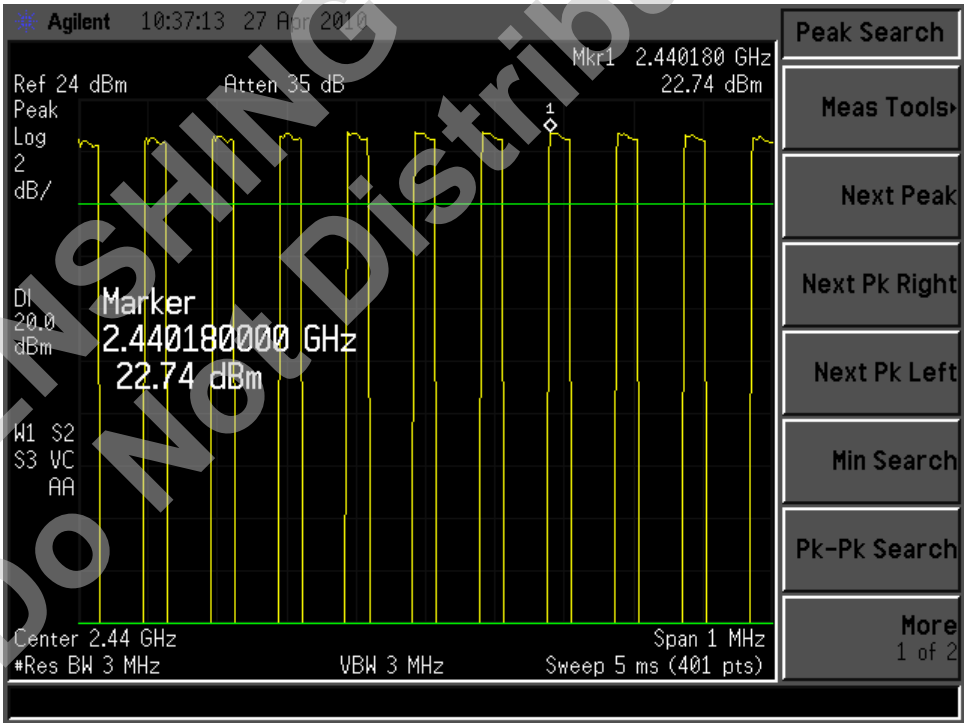


Timing of Enhanced ShockBurst™ for one packet upload (2Mbps)

Communication Example 2: When transferring date to 2.4GHz, the Length is XX; REGISTER is shown from table below:

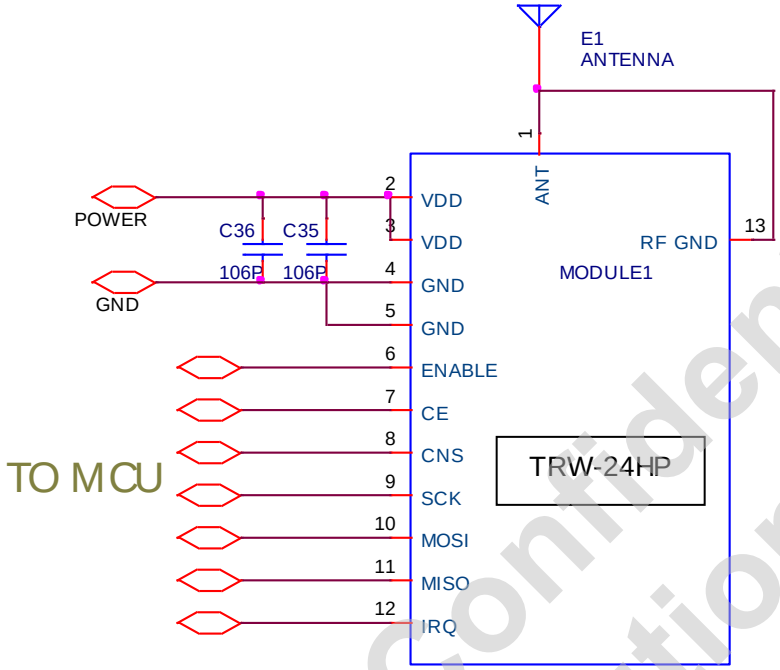
Address	00	01	02	03	04	05	06	07
Data								
Address	08	09	0A	0B	0C	0D	0E	0F
Data								
Address	10	11	12	13	14	15	16	17
Data								
Address	18	19	1A	1B	1C	1D		
Data								

Output Power



Layout Notes

- It should be to add several big capacitors before power on to increase stable RF communication.



- It should not run digital signal at end of module to avoid EMI transmitted to RF module.
- Module add external antenna, the bottom part of the PCB antenna should be as much as possible to provide non- copper park area for the antenna radiation use.
- Please notice, if you used termial inside the module to connect with external antenna, ANT PIN & RF GND PIN don't solder on PCB.